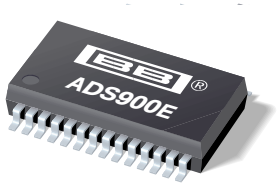
BURR - BROWN®



ADS900

10-Bit, 20MHz +3V Supply ANALOG-TO-DIGITAL CONVERTER

FEATURES

- +2.7V TO +3.7V SUPPLY OPERATION
- INTERNAL REFERENCE
- LOW POWER: 52mW at +3V
- SINGLE-ENDED INPUT RANGE: 1V to 2V
- WIDEBAND TRACK/HOLD: 350MHz
- 28-PIN SSOP PACKAGE

APPLICATIONS

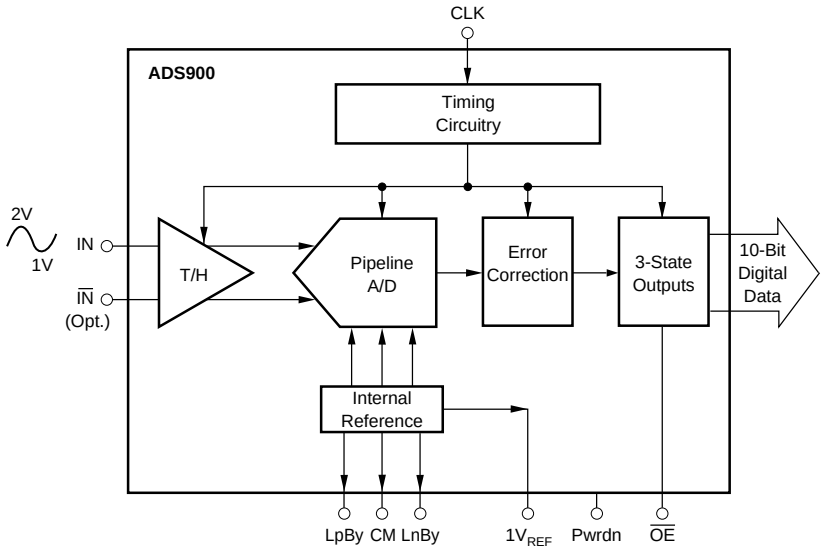
- PORTABLE INSTRUMENTATION
- IF AND BASEBAND COMMUNICATIONS
- CABLE MODEMS
- SET-TOP BOXES
- PORTABLE TEST EQUIPMENT
- COMPUTER SCANNERS

DESCRIPTION

The ADS900 is a high speed pipelined analog-to-digital converter. This complete converter includes a high bandwidth track/hold, a 10-bit quantizer and an internal reference.

The ADS900 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for telecommunications, video and test instrumentation applications.

This high performance A/D converter is specified for performance at a 20MHz sampling rate. The ADS900 is available in a 28-pin SSOP package.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

At T_A = +25°C, V_S = +3V, Single-Ended Input, Sampling Rate = 20MHz, unless otherwise specified.

PARAMETER	CONDITIONS	TEMP	ADS900E MIN	ADS900E TYP	ADS900E MAX	UNITS
Resolution			10			Bits
Specified Temperature Range	Ambient Air		–40		+85	°C
ANALOG INPUT						
Single-Ended Full Scale Input Range (1Vp-p)				1.0 to 2.0		V
Differential Full Scale Input Range (0.5Vp-pX 2)				1.25 to 1.75		V
Common-Mode Voltage				1.5		V
Analog Input Bias Current				1		µA
Input Impedance				1.25 || 5		MΩ || pF
DIGITAL INPUTS		Full				
Logic Family				TTL/HCT COMPATIBLE CMOS		
High Input Voltage, V_{IH}			2.0		V_{DD}	V
Low Input Voltage, V_{IL}					0.8	V
High Input Current, I_{IH}				±10		µA
Low Input Current, I_{IL}				±10		µA
Input Capacitance				5		pF
CONVERSION CHARACTERISTICS						
Start Conversion				RISING EDGE OF CONVERT CLOCK		
Sample Rate		Full	10k		20M	Samples/s
Data Latency				5		Clk Cyc
DYNAMIC CHARACTERISTICS						
Differential Linearity Error						
f = 500kHz (Largest Code Error)		Full		±0.7	±1.0	LSBs
f = 10MHz (Largest Code Error)		Full		±0.7	±1.0	LSBs
No Missing Codes		Full		Guaranteed		
Integral Nonlinearity Error, f = 500kHz		Full		±3.5		LSBs
Spurious Free Dynamic Range[1]						
f = 500kHz (–1db input)		Full	47	53		dBFS[2]
		+25°C	49	53		dBFS
f = 10MHz (–1dB input)		Full	47	53		dBFS
		+25°C	48	53		dBFS
Two-Tone Intermodulation Distortion[3]						
f = 4.5MHz and 5.0MHz (–7dB each tone)		+25°C		50		dBc
Signal-to-Noise Ratio (SNR)						
f = 500kHz (–1dB input)		Full	45	49		dB
		+25°C	46	50		dB
f = 10MHz (–1dB input)		Full	45	49		dB
		+25°C	46	50		dB
Signal-to-(Noise + Distortion) (SINAD)						
f = 500kHz (–1dBFS input)		Full	44	48		dB
		+25°C	45	48		dB
f = 3.58MHz (–1dBFS input)		Full	44	48		dB
		+25°C	45	48		dB
f = 10MHz (–1dBFS input)		Full	44	48		dB
		+25°C	45	48		dB
Differential Gain Error	NTSC, PAL			2.3		%
Differential Phase Error	NTSC, PAL			1		degrees
Output Noise	Input Grounded			0.2		LSBs rms
Aperture Delay Time				2		ns
Aperture Jitter				7		ps rms
Analog Input Bandwidth						
Small Signal	–20dBFS Input	+25°C		350		MHz
Full Power	0dBFS Input	+25°C		100		MHz
Overvoltage Recovery Time[6]	1.5X FS Input	+25°C		2		ns
DIGITAL OUTPUTS	C_L = 15pF	Full				
Logic Family				TTL/HCT COMPATIBLE CMOS		
Logic Coding				SOB		
High Output Voltage, V_{OH}			2.4		V_{DD}	V
Low Output Voltage, V_{OL}					0.4	V
3-State Enable Time	$\overline{OE}$ = L	Full		20	40	ns
3-State Disable Time	$\overline{OE}$ = H			2	10	ns
Internal Pull-Down				50		kΩ
Power-Down Enable Time	PwrDn = L			133		ns
Power-Down Disable Time	PwrDn = H			18		ns
Internal Pull-Down				50		kΩ

SPECIFICATIONS (CONT)

At T_A = +25°C, V_S = +3V, Single-Ended Input, Sampling Rate = 20MHz, unless otherwise specified.

PARAMETER	CONDITIONS	TEMP	ADS900E MIN	ADS900E TYP	ADS900E MAX	UNITS
ACCURACY						
Gain Error		+25°C		8	10	%FS
Input Offset	Referred to Ideal Midscale	Full		15	60	mV
Power Supply Rejection (Gain)	ΔV_S = +10%	Full	42	55		dB
Power Supply Rejection (Offset)		Full	42	62		dB
Internal Positive Reference Voltage		Full		+1.75		V
Internal Negative Reference Voltage		Full		+1.25		V
POWER SUPPLY REQUIREMENTS						
Supply Voltage: $+V_S$	Operating	Full	+2.7	+3	+3.7	V
Supply Current: $+I_S$	Operating	Full		18	22	mA
Power Dissipation	Operating, +3V	Full		54	66	mW
		25°C		52		mW
Power Dissipation (Power Down)	Operating, +3V	Full		10		mW
Thermal Resistance, θ_{JA}						
28-Pin SSOP				50		°C/W

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to full scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) No rollover of bits.

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	$+V_S$, +0.3V
Logic Input	$+V_S$, +0.3V
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
ADS900E	28-Pin SSOP	324	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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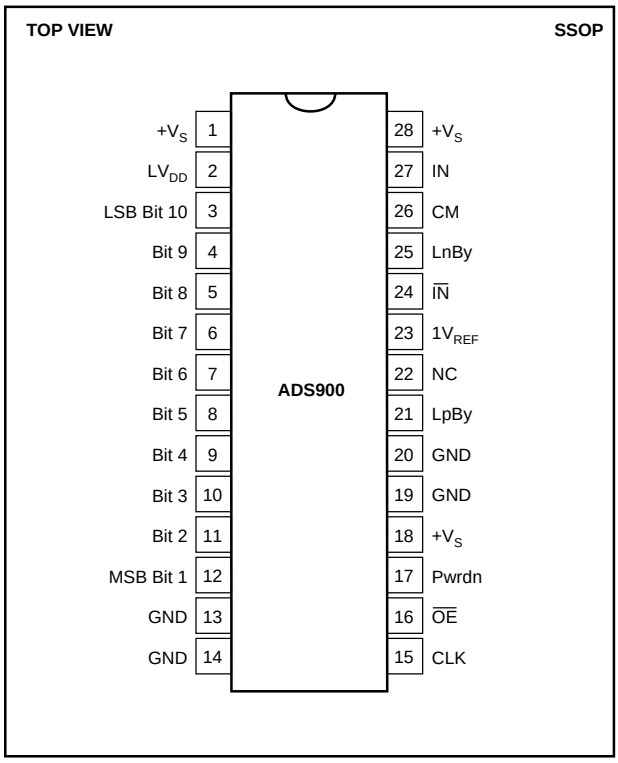
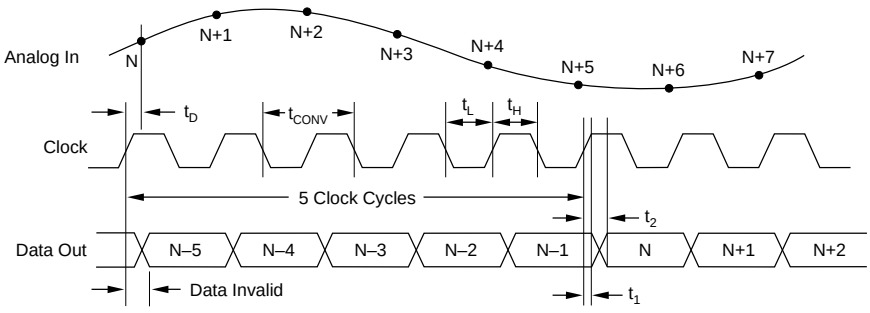
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	$+V_S$	Analog Supply
2	LV_{DD}	Logic Supply Voltage
3	Bit 10	Data Bit 10 (LSB)
4	Bit 9	Data Bit 9
5	Bit 8	Data Bit 8
6	Bit 7	Data Bit 7
7	Bit 6	Data Bit 6
8	Bit 5	Data Bit 5
9	Bit 4	Data Bit 4
10	Bit 3	Data Bit 3
11	Bit 2	Data Bit 2
12	Bit 1	Data Bit 1 (MSB)
13	GND	Analog Ground
14	GND	Analog Ground
15	CLK	Convert Clock Input
16	$\overline{OE}$	Output Enable, Active Low
17	Pwrdn	Power Down Pin
18	$+V_S$	Analog Supply
19	GND	Analog Ground
20	GND	Analog Ground
21	LpBy	Positive Ladder Bypass
22	NC	No Connection
23	$1V_{REF}$	1V Reference Output
24	$\overline{IN}$	Complementary Input
25	LnBy	Negative Ladder Bypass
26	CM	Common-Mode Voltage Output
27	IN	Analog Input
28	$+V_S$	Analog Supply

TIMING DIAGRAM

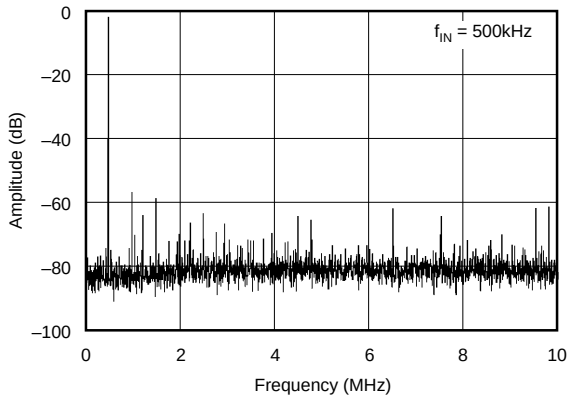


SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	50		100µs	ns
t_L	Clock Pulse Low	24	25		ns
t_H	Clock Pulse High	24	25		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12	ns

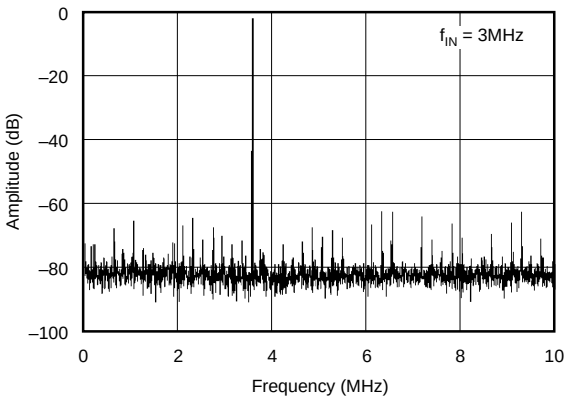
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = +3V, Single-Ended Input, Sampling Rate = 20MHz, unless otherwise specified.

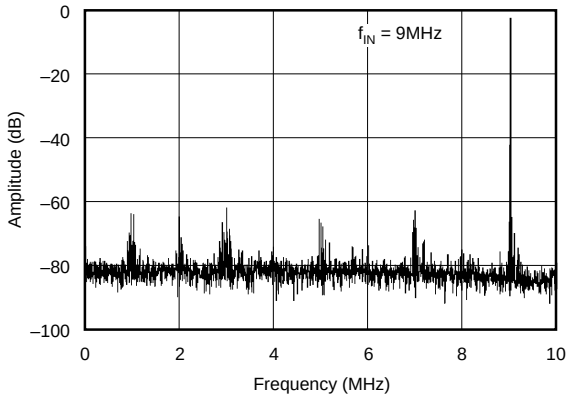
SPECTRAL PERFORMANCE



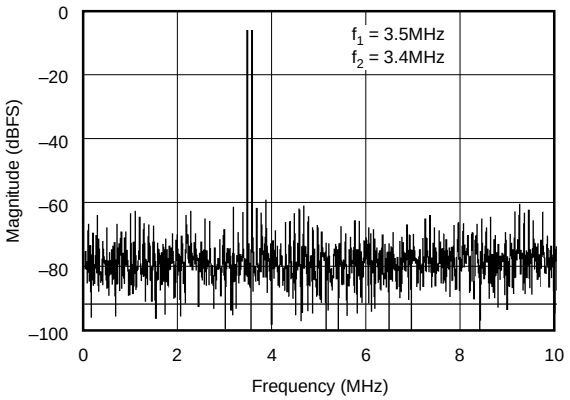
SPECTRAL PERFORMANCE



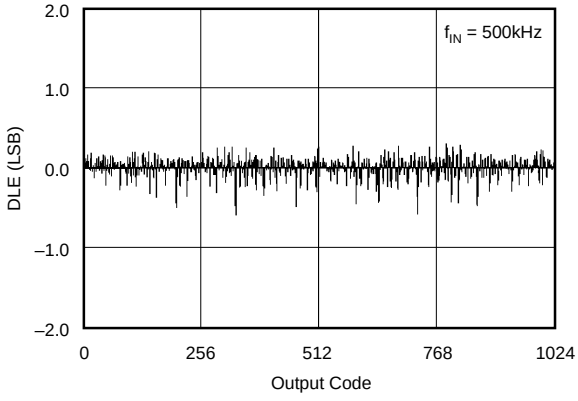
SPECTRAL PERFORMANCE



TWO-TONE INTERMODULATION



DIFFERENTIAL LINEARITY ERROR



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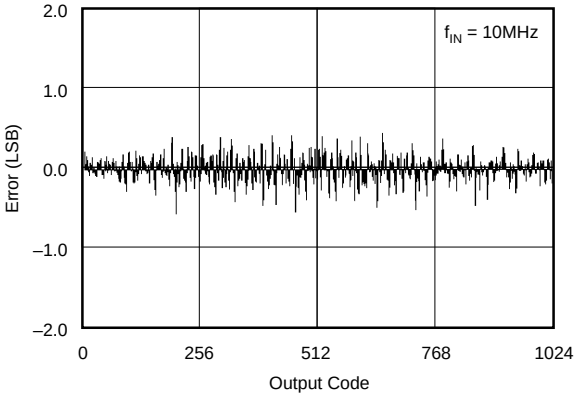
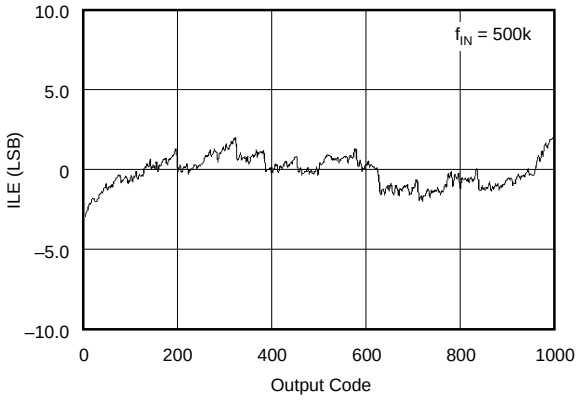


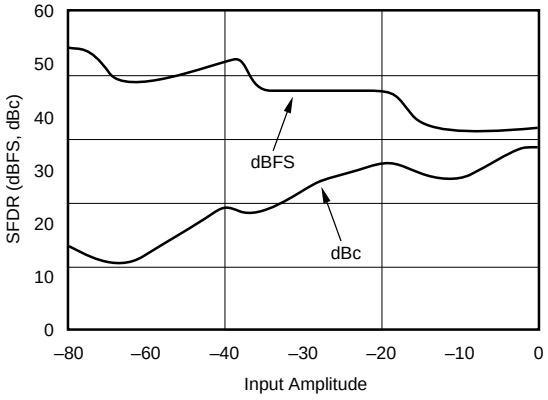
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +3V, Single-Ended Input, Sampling Rate = 20MHz, unless otherwise specified.

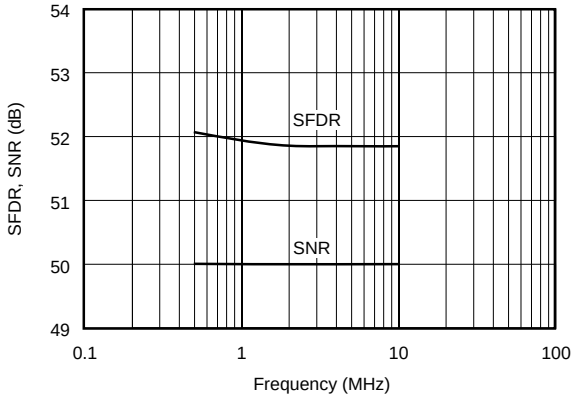
INTEGRAL LINEARITY ERROR



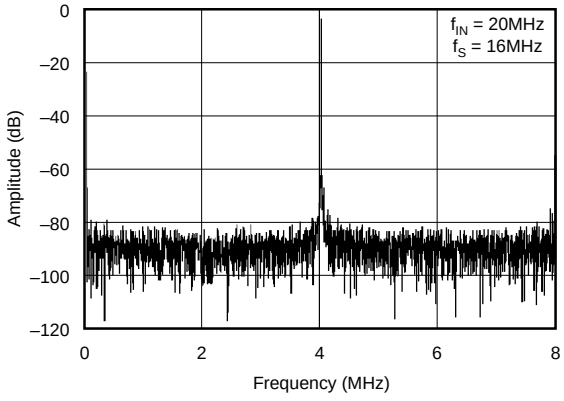
SWEPT POWER SFDR



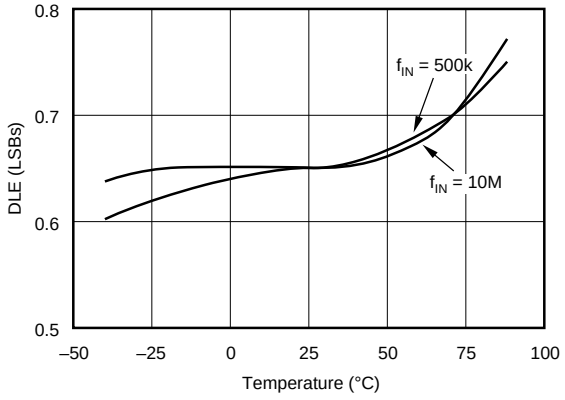
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



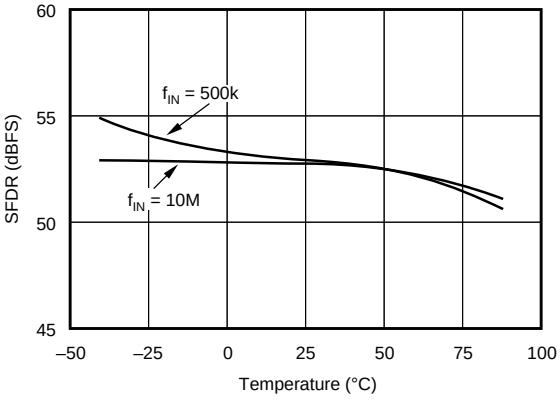
UNDERSAMPLING (With Differential Input)



DIFFERENTIAL LINEARITY ERROR
vs TEMPERATURE



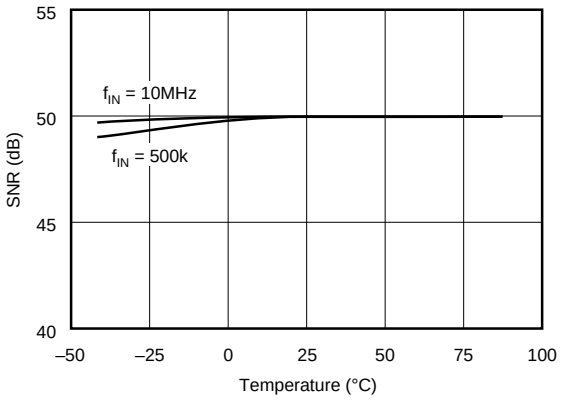
SPURIOUS FREE DYNAMIC RANGE (SFDR)
vs TEMPERATURE



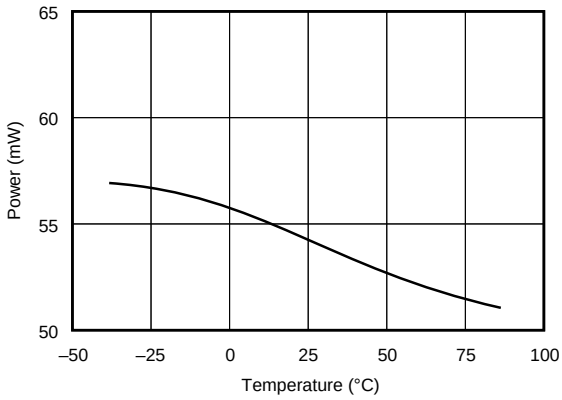
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +3V, Single-Ended Input, Sampling Rate = 20MHz, unless otherwise specified.

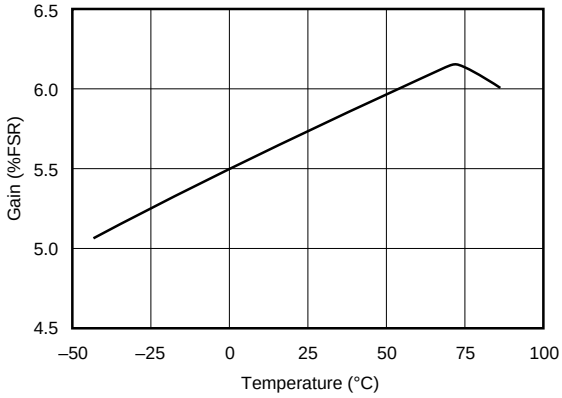
SIGNAL-TO-NOISE RATIO (SNR) vs TEMPERATURE



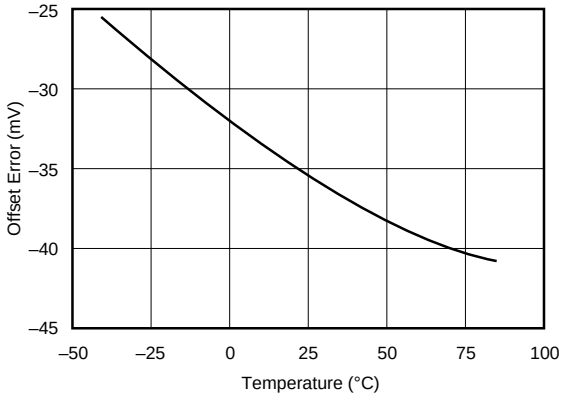
POWER DISSIPATION vs TEMPERATURE



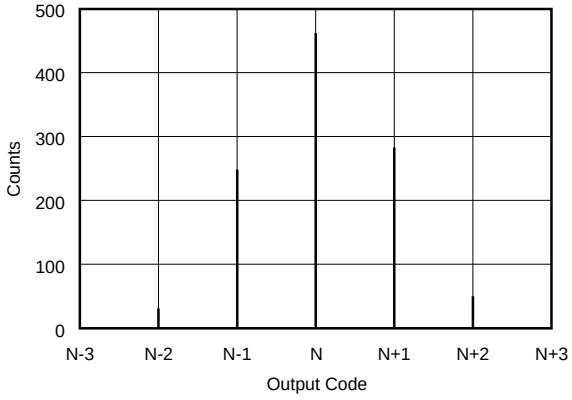
GAIN ERROR vs TEMPERATURE



OFFSET ERROR vs TEMPERATURE



OUTPUT NOISE HISTOGRAM (DC Input)



THEORY OF OPERATION

The ADS900 is a high speed sampling analog-to-digital converter that utilizes a pipeline architecture. The fully differential topology and digital error correction guarantee 10-bit resolution. The track/hold circuit is shown in Figure 1. The switches are controlled by an internal clock which has a non-overlapping two phase signal, $\phi1$ and $\phi2$. At the sampling time the input signal is sampled on the bottom plates of the input capacitors. In the next clock phase, $\phi1$, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time the charge redistributes between C_I and C_H, completing one track/hold cycle. The differential output is a held DC representation of the analog input at the sample time. In the normal mode of operation, the complementary input is tied to the common-mode voltage. In this case, the track/hold circuit converts a single-ended input signal into a fully differential signal for the quantizer. Consequently, the input signal gets amplified by a gain or two, which improves the signal-to-noise performance. Other parameters such as small-signal and full-power bandwidth, and wideband noise are also defined in this stage.

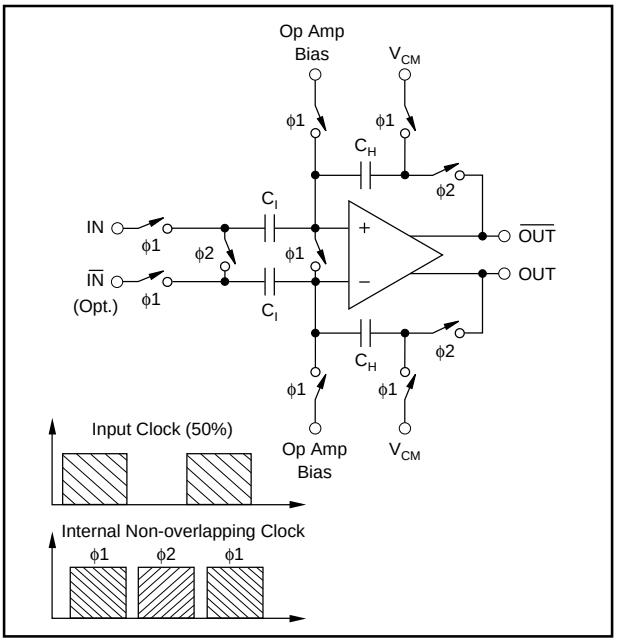


FIGURE 1. Input Track/Hold Configuration with Timing Signals.

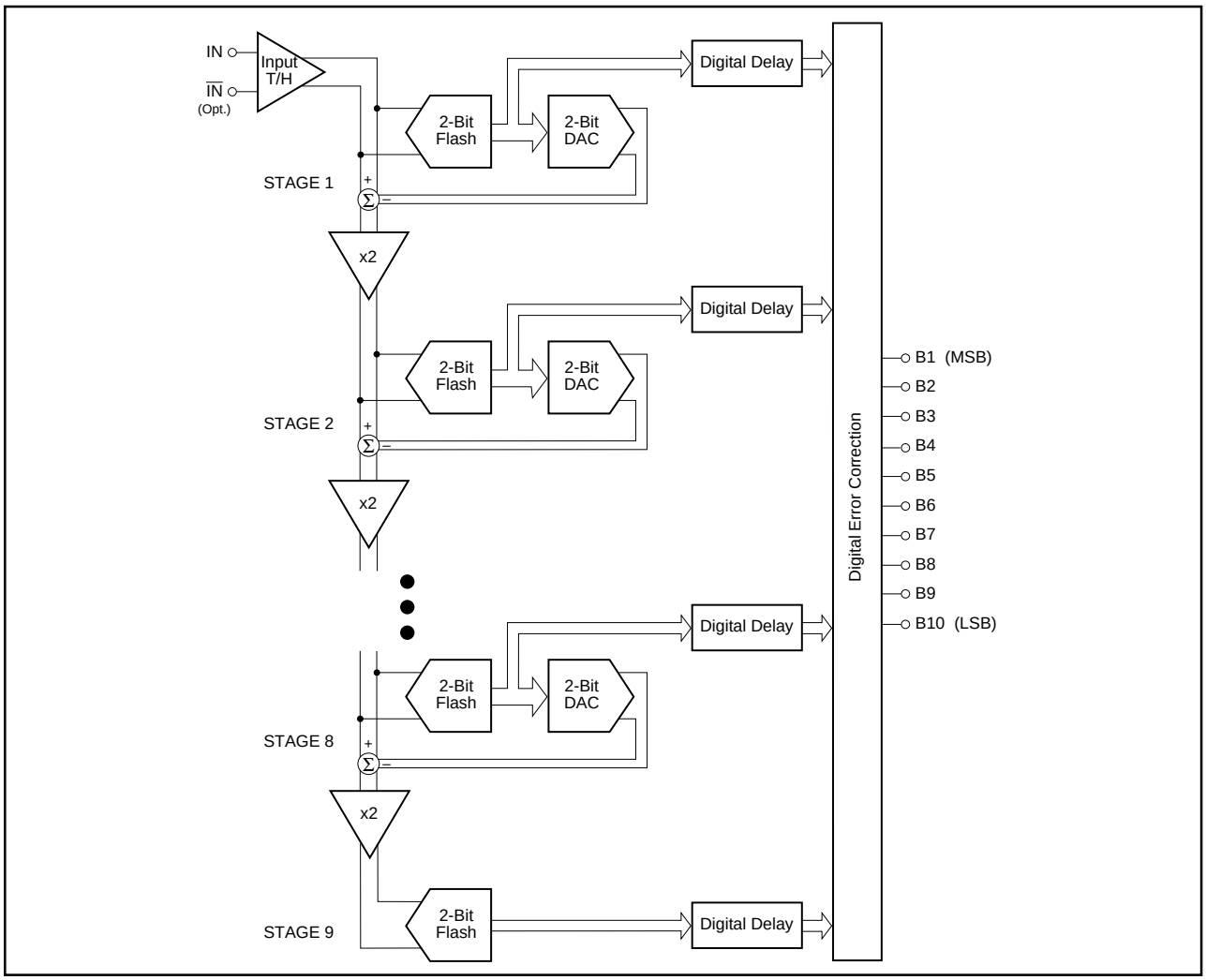


FIGURE 2. Pipeline A/D Architecture.

The pipelined quantizer architecture has 9 stages with each stage containing a two-bit quantizer and a two bit digital-to-analog converter, as shown in Figure 2. Each two-bit quantizer stage converts on the edge of the sub-clock, which is the same frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to time-align it with the data created from the following quantizer stages. This aligned data is fed into a digital error correction circuit which can adjust the output data based on the information found on the redundant bits. This technique provides the ADS900 with excellent differential linearity and guarantees no missing codes at the 10-bit level.

The ADS900 includes an internal reference circuit that provides the bias voltages for the internal stages (for details see "Internal Reference"). A midpoint voltage is established by the built-in resistor ladder that is made available at pin 26 "CM". This voltage can be used to bias the inputs up to the recommended common-mode voltage or used to level shift the input driving circuitry. The ADS900 can be used in both a single-ended or differential input configuration. When operated in single-ended mode, the reference midpoint (pin 26) should be tied to the inverting input, pin 24.

To accommodate a bipolar signal swing, the ADS900 operates with a common-mode voltage (V_{CM}) which is derived from the internal references. Due to the symmetric resistor ladder inside the ADS900, the V_{CM} is situated between the top and bottom reference voltage. Equation (1) can be used for calculating the common-mode voltage level.

$$V_{CM} = (REFT + REFB)/2 \quad (1)$$

DIGITAL OUTPUT DATA

The 10-bit output data is provided at CMOS logic levels. There is a 5.0 clock cycle data latency from the start convert signal to the valid output data. The standard output coding is Straight Offset Binary where a full scale input signal corresponds to all "1's" at the output. The digital outputs of the ADS900 can be set to a high impedance state by driving the $\overline{OE}$ (pin 16) with a logic "HI". Normal operation is achieved with pin 16 "LO" or Floating due to internal pull-down resistors. This function is provided for testability purposes but is not recommended to be used dynamically. The capacitive loading on the digital outputs should be kept below 15pF.

SINGLE-ENDED INPUT ($\overline{IN}$ = 1.5V DC)	STRAIGHT OFFSET BINARY (SOB) PIN 12 FLOATING or LO
+FS (IN = +2V)	1111111111
+FS –1LSB	1111111111
+FS –2LSB	1111111110
+3/4 Full Scale	1110000000
+1/2 Full Scale	1100000000
+1/4 Full Scale	1010000000
+1LSB	1000000001
Bipolar Zero (IN +1.5V)	1000000000
–1LSB	0111111111
–1/4 Full Scale	0110000000
–1/2 Full Scale	0100000000
–3/4 Full Scale	0010000000
–FS +1LSB	0000000001
–FS (IN = +1V)	0000000000

TABLE I. Coding Table for the ADS900.

APPLICATIONS

DRIVING THE ANALOG INPUTS

Figure 3 shows an example of an ac-coupled, single-ended interface circuit using high-speed op amps that operate on dual supplies (OPA650, OPA658). The common-mode reference voltage (V_{CM}), here +1.5V, biases the bipolar, ground-referenced input signal. The capacitor C_1 and resistor R_1 form a high-pass filter with the –3dB frequency set at

$$f_{-3dB} = 1/(2 \pi R_1 C_1) \quad (2)$$

The values for C_1 and R_1 are not critical in most applications and can be set freely. The values shown correspond to a –3dB corner frequency of 1.6kHz.

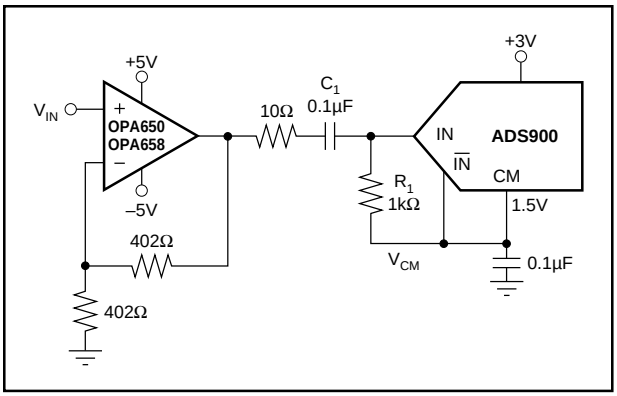


FIGURE 3. AC-Coupled Driver.

Figure 4 depicts a circuit that can be used in single-supply applications. The common-mode voltage biases the op amp up to the appropriate common-mode voltage, for example V_{CM} = +1.5V. With the use of capacitor C_G the DC gain for the non-inverting op amp input is set to +1V/V. As a result the transfer function is modified to

$$V_{OUT} = V_{IN} \{(1 + R_F/R_G) + V_{CM}\} \quad (3)$$

Again, the input coupling capacitor C_1 and resistor R_1 form a high-pass filter. At the same time the input impedance is defined by R_1. Possible op amps are CLC450, EL2150 and LM6152. Resistor R_S isolates the op amp's output from the capacitive load to avoid oscillation. It can also be used to establish a defined roll-off for the wideband noise. Its value is usually between 10Ω and 100Ω.

DIFFERENTIAL MODE OF OPERATION

Some minor performance improvements in SFDR and THD can be realized by operating the ADS900 in its optional differential configuration. A RF-transformer with a center tap provides the best method of performing a single-ended to differential conversion and interface directly to the ADS900.

As a passive component, a transformer can be used to step-up the signal amplitude without adding noise or distortion. At the same time it electrically isolates the front-end from the converter. In order to achieve optimum performance and to bias the converter inputs up to the correct common-mode voltage the mid-reference pin "CM" can be tied directly to the center tap of the transformer.

Figure 6 shows an example for a single-ended DC-coupled interface circuit using one high-speed op amp to level-shift the ground-referenced input signal to condition it for the input requirements of the ADS900. With a +3V supply the input signal swings 1Vp-p centered around a typical common-mode voltage of +1.5V. This voltage can be derived from the internal bottom reference (REFB = +1.25V) and then fed back through a resistor divider (R_1, R_2) to level shift the driving op amp (A_1). A capacitor across R_2 will shunt most of the wideband noise to ground. Depending on the configured gain the values of resistors R_1 and R_2 must be adjusted since the offsetting voltage (V_{OS}) is amplified by the non-inverting gain, $1+(R_F/R_{IN})$. This example assumes the sum of R_1 and R_2 to be 5kΩ, drawing only 250µA from the bottom reference. Considerations for the selection of a

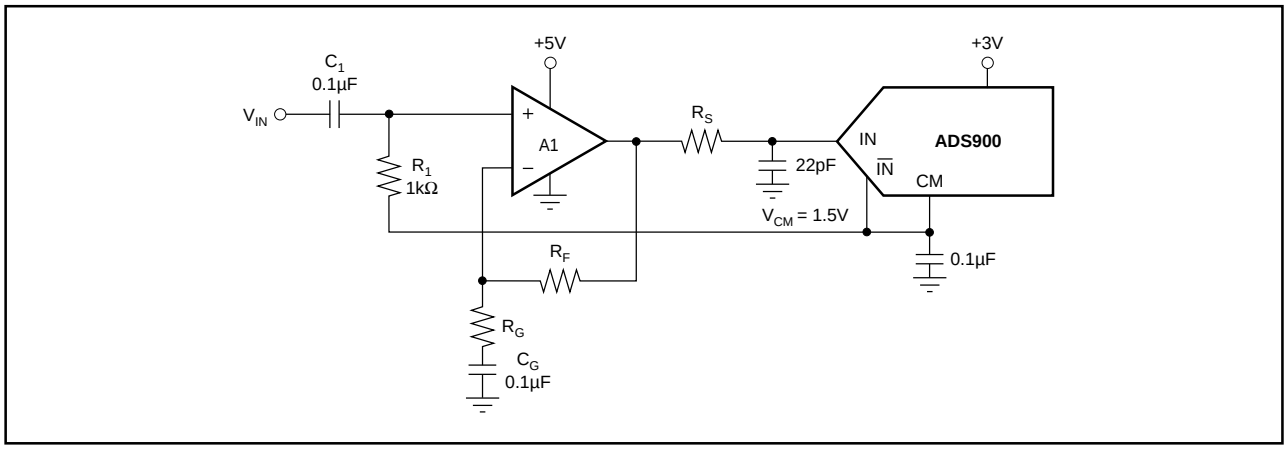


FIGURE 4. Driver Circuit Using Single Supply.

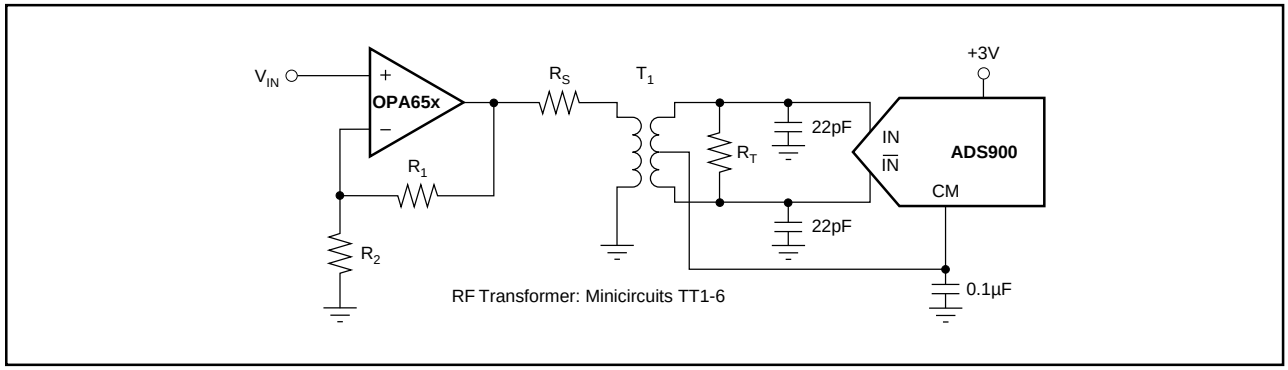


FIGURE 5. Single-Ended to Differential Drive Circuit Using a Transformer.

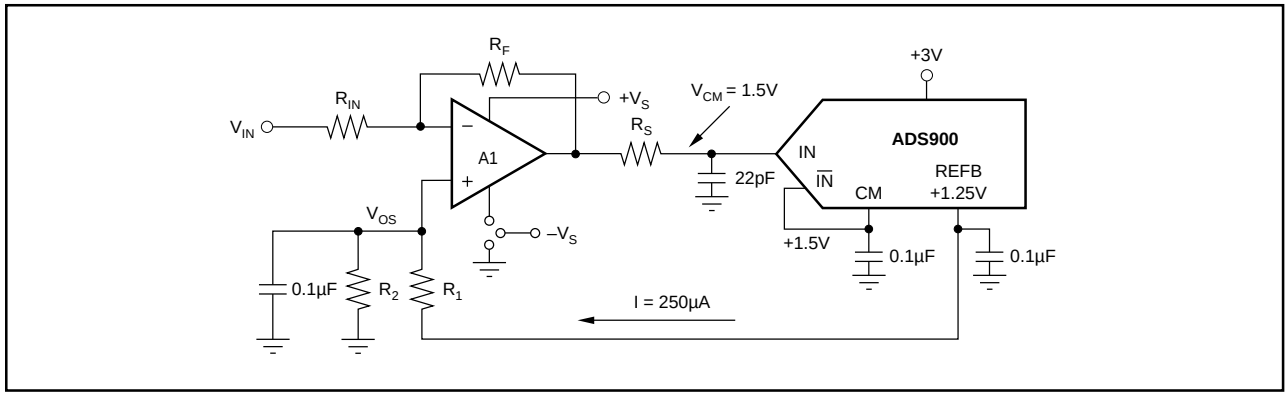


FIGURE 6. Single-Ended DC-Coupled Input Circuit.

proper op amp should include its output swing, input common-mode range, and bias current. It should be noted that any DC voltage difference between the inputs, IN and $\overline{IN}$, will show up as an offset at the output. At the same time an offset adjustment can be accomplished.

INTERNAL REFERENCE

The ADS900 features an internal pipeline reference that provides fixed reference voltages for the internal stages. As shown in Figure 7 a buffer for each the top and bottom reference is connected to the resistor ladder, which has a nominal resistance of 4kΩ (±15%). The two outputs of the buffers are brought out at pin 21 (LpBy) and pin 25 (LnBy), primarily to connect external bypass capacitors, typically 0.1µF, which will improve the performance. The buffers can drive limited external loads, for example for level shifting of the converter's interface circuit, however, the current draw should be limited to approximately 1mA.

Derived from the top reference of +1.75V is an additional voltage of +1.0V. Note that this voltage, available on pin 23, is not buffered and care should be taken when external loads are applied. In normal operation, this pin is left unconnected and no bypassing components are required.

CLOCK INPUT REQUIREMENTS

The clock input of the ADS900 is designed to accommodate either +5V or +3V CMOS logic levels. To drive the clock input with a minimum amount of duty cycle variation and support maximum sampling rates (20Msps) high speed or advanced CMOS logic should be used (HC/HCT, AC/ACT). When digitizing at high sampling rates, a 50% duty cycle along with fast rise and fall times (2ns or less) are recommended to meet the rated performance specifications. However, the ADS900 performance is tolerant to duty cycle variations of as much as ±10% without degradation. For applications operating with input frequencies up to Nyquist or undersampling applications, special considerations must be made to provide a clock with very low jitter. Clock jitter leads to aperture jitter (t_A) which can be the ultimate limitation in achieving good SNR performance. Equation (4) shows the relationship between aperture jitter, input frequency and the signal-to-noise ratio:

$$SNR = 20\log10\ [1/(2\ \pi\ f_{IN}\ t_A)] \qquad (4)$$

For example, in the case of a 10MHz full-scale input signal and an aperture jitter of t_A = 20ps the SNR is clock jitter limited to 58dB.

DIGITAL OUTPUTS

The digital outputs of the ADS900 are standard CMOS stages and designed to be compatible to both high speed TTL and CMOS logic families. The logic thresholds are for low-voltage CMOS: V_{OL} = 0.4V, V_{OH} = 2.4V, which allows the ADS900 to directly interface to 3V-logic. The digital outputs of the ADS900 uses a dedicated digital supply pin (pin 2, LV_{DD}) see Figure 8. By adjusting the voltage on LV_{DD}, the digital output levels will vary respectively. It is recommended to limit the fan-out to one to keep the capacitive loading on the data lines below the specified 15pF. If necessary, external buffers or latches may be used that provide the added benefit of isolating the A/D converter from any digital activities on the bus coupling back high frequency noise and degrading the performance.

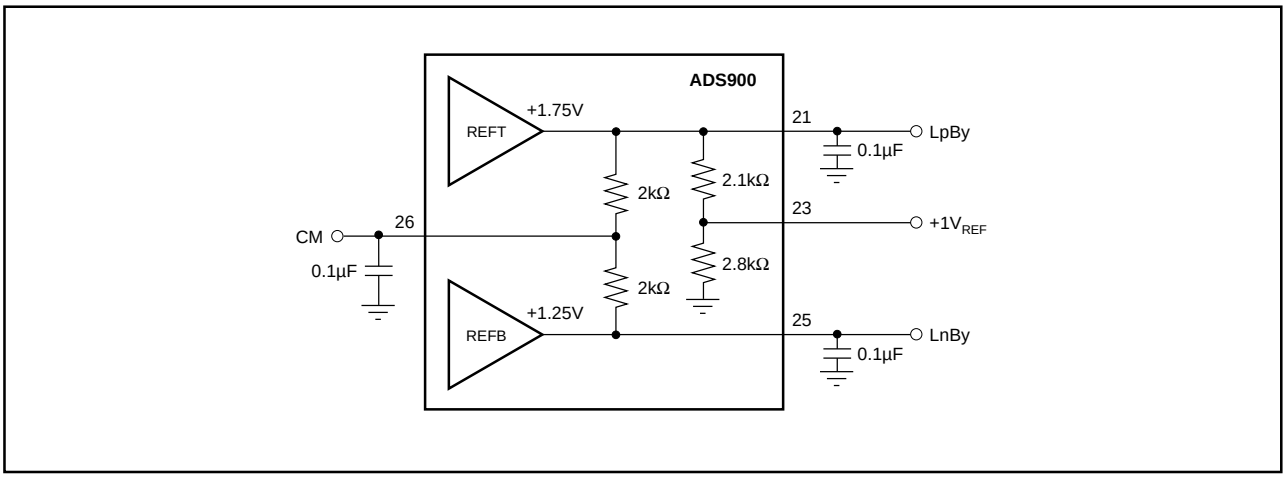


FIGURE 7. Internal Reference Structure and Recommended Reference Bypassing.

POWER-DOWN MODE

The ADS900's low power consumption can be reduced even further by initiating a power down mode. For this, the Power Down Pin (Pin 17) must be tied to a logic "High" reducing the current drawn from the supply by about 70%. In normal operation the power-down mode is disabled by an internal pull-down resistor (50kΩ).

During power-down the digital outputs are set in 3-state. With the clock applied, the converter does not accurately process the sampled signal. After removing the power-down condition the output data from the following 5 clock cycles is invalid (data latency).

DECOUPLING AND GROUNDING CONSIDERATIONS

The ADS900 has several supply pins, one of which is dedicated to only supply the output driver (LV_{DD}). The remaining supply pins are not divided into analog and digital supply pins since they are internally connected on the chip. For this reason it is recommended to treat the converter as an analog component and to power it from the analog supply only. Digital supply lines often carry high levels of noise which can couple back into the converter and limit performance.

Because of its fast switching architecture, the converter also generates high frequency transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently bypassed. Figure 9 shows the recommended decoupling scheme for the analog supplies. In most cases 0.1µF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore they should be located as close to the supply pins are possible.

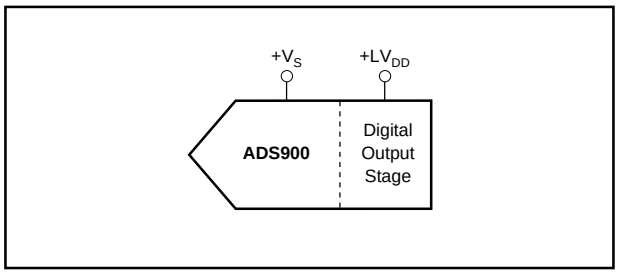


FIGURE 8. Independent Supply Connection for Output Stage.

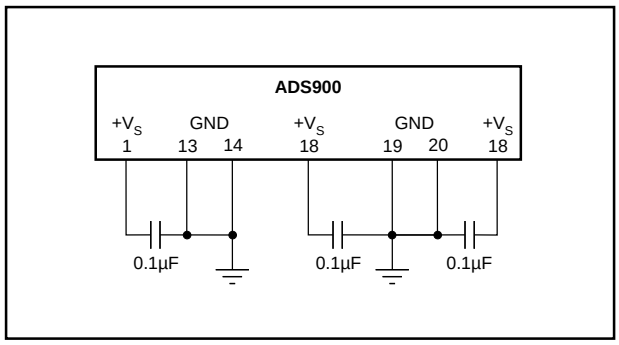


FIGURE 9. Recommended Bypassing for Analog Supply Pins.